

125mW Direct Drive Line Drivers/Headphone Amplifiers

FEATURES

- Direct Drive Outputs Eliminate DC-Blocking Capacitors, Save Space
- Excellent Bass Fidelity
- Shutdown and Startup without any Click-Pop Noise
- Exceptional Low THD+N: 0.001% Minimum
- Absolutely Low Noise and High SNR Performance, V_N : 7 μ V, SNR: 112dB
- Differential or Single-Ended Input
- Wide 2.5V to 5.5V Operating Range
- Output Power: 125mW ($f_{IN} = 1$ kHz, $V_{DD}=5$ V, $R_L=32\Omega$, THD+N=1%);
- Output Voltage Swing:
 - 3Vrms ($f_{IN} = 1$ kHz, $V_{DD}=5$ V, $R_L=1$ k Ω , THD+N<0.1%);
 - 2Vrms ($f_{IN} = 1$ kHz, $V_{DD}=5$ V, $R_L=600\Omega$, THD+N<0.1%);
- Pb Free Packages, QFN16L-PP 3mm*3mm, Extremely Simple BOM Needed

APPLICATIONS

- Headphones · Simple Multimedia Interfaces
- Set-Top Boxes · Blue-ray and DVD Players
- LCD Televisions · Prosumer Audio Devices

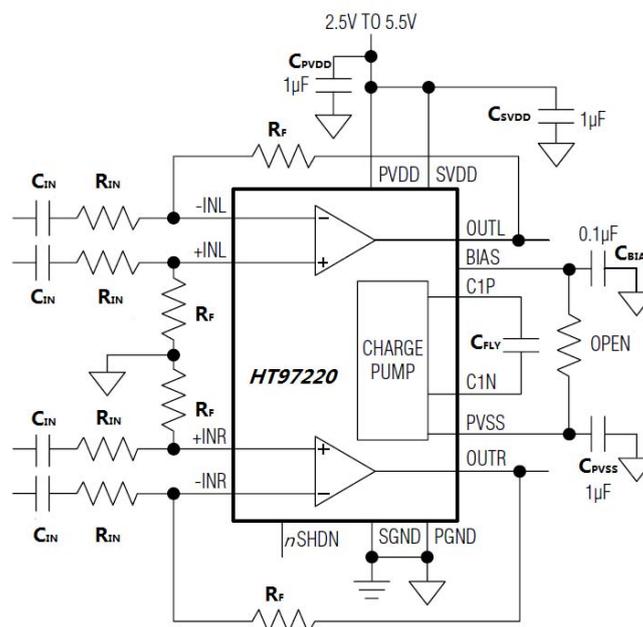
DESCRIPTION

The HT97220 is a differential input Direct Drive line driver/headphone amplifier, which can also drive single-ended input signal. It is capable of driving line level loads with 3VRMS into 1k Ω with a 5V supply and 2VRMS into 600 Ω loads from a 3.3V supply. A headphone load is capable of being driven with 125mW into 32 Ω with a 5V supply. The IC is offered with an externally set gain through external resistors (or an internally fixed 6dB gain which needs to be pre-booked). The external gain setting nodes can also be used to configure filters for set-top box applications. The IC has exceptional THD+N over the full audio bandwidth.

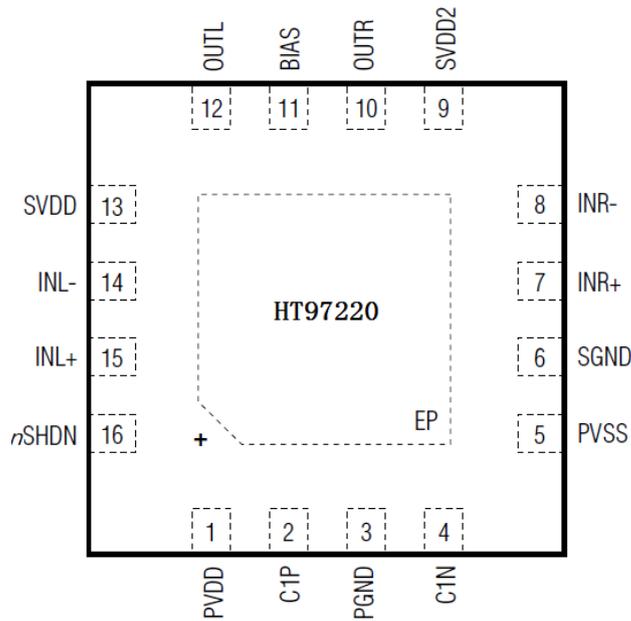
Two versions of the IC can be chosen with different turn-on times (t_{ON}). The versions for headphone applications feature a t_{ON} of 5.5ms while the version, intended for set-top-box applications, which needs to be pre-booked, feature a 130ms t_{ON} . An on-chip charge pump inverts the power-supply input, creating a negative rail. The output stage of the amplifier is powered between the positive input supply and the output of the charge pump. The bipolar supplies bias the output about ground, eliminating the need for large, distortion-introducing output coupling capacitors. The IC shutdowns and startups without click-pop noise.

The IC is available in a 3mm x 3mm, 16-pin QFN-PP and is specified over the extended -40 $^{\circ}$ C to +85 $^{\circ}$ C temperature range.

TYPICAL APPLICATION



■ TERMINAL CONFIGURATION



■ TERMINAL FUNCTION

PIN	NAME	Description
1	PVDD	Charge-Pump Power-Supply Input. Bypass to PGND with 1 μ F.
2	C1P	Positive Flying Capacitor Connection. Connect a 0.47 μ F capacitor between C1P and C1N.
3	PGND	Power Ground. Connect PGND and SGND together at the system ground plane.
4	C1N	Negative Flying Capacitor Connection. Connect a 0.47 μ F capacitor between C1P and C1N.
5	PVSS	Negative Charge-Pump Output. Bypass to PGND with 1 μ F.
6	SGND	Signal Ground. Connect PGND and SGND together at the system ground plane.
7	INR+	Right Positive Polarity Input
8	INR-	Right Negative Polarity Input
9	SVDD2	Signal Path Power-Supply Input. Bypass to PGND with 1 μ F. Connect directly to PVDD.
10	OUTR	Right Direct Drive Output
11	BIAS	Internal Supply Node. Bypass to PGND with 0.1 μ F.
12	OUTL	Left Direct Drive Output
13	SVDD	Signal Path Power-Supply Input. Bypass to PGND with 1 μ F. Connect directly to PVDD.
14	INL-	Left Negative Polarity Input
15	INL+	Left Positive Polarity Input
16	nSHDN	Active-Low Shutdown. Drive nSHDN high for normal operation.
—	EP	Exposed Pad. Electrically connect to PGND or leave unconnected.

ORDERING INFORMATION

Part Number	Package Type	Marking	Operating Temperature Range	MOQ/Shipping Package
HT97220	QFN16L-PP	HT97220 UVWXYZ *1	-40°C ~ 85°C	Tape & Reel 5000PCS

*1 WXYZ/UVWXYZ is production track code.

ELECTRICAL CHARACTERISTIC
Absolute Maximum Ratings*2

PARAMETER*3	Symbol	MIN	MAX	UNIT
Supply Voltage (SVDD, SVDD2, PVDD) Range	V _{DD}	-0.3	+6.0	V
PVSS and BIAS Voltage Range		-6.0	+0.3	V
SGND Voltage Range	SGND	-0.3	+0.3	V
Input (INL+, INL-, INR+, INR-) Voltage Range	V _{IN}	-V _{SVDD} /2	+V _{SVDD} /2	V
Input (nSHDN) Voltage Range	nSHDN	-0.3	+6	V
Output (OUTL, OUTF) Voltage Range	V _{OUT}	-4.5	4.5	V
C1P Voltage Range	C1P	-0.3	V _{PVDD} +0.3	V
C1N Voltage Range	C1N	V _{PVSS}	+0.3	V
Operating temperature range	TA	-40	85	°C
Operating junction temperature range	TJ	-40	150	°C
Storage temperature range	TSTG	-65	150	°C

*2 Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*3 All Voltages is referenced to PGND.

Electrical Characteristics*4

Condition: Ta=25°C, V_{DD} (= V_{PVDD} = V_{SVDD} = V_{SVDD2}) = 5.0V, V_{PGND} = V_{SGND} = 0V, R_{IN} = R_F = 20kΩ, C_{FLY} = 0.47μF, C_{PVDD} = C_{PVSS} = 1μF, C_{BIAS} = 0.1μF, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply voltage range	V _{DD}		2.5		5.5	V
Quiescent Supply Current	I _{DD}	No Load		5.0		mA
Under-voltage Lockout	UVLO				2.2	V
Shutdown Supply Current	I _{SD}	nSHDN = 0		1	10	μA
Start-up time	t _{ON}			4.2		ms
Amplifier						
Output Offset Voltage	V _{OS}				350	μV
Input Common-Mode Voltage Range	V _{CM}	Voltage at IN+ and IN-	-0.5 x V _{PVDD}		+0.5 x V _{PVDD}	V
Maximum Differential Input Signal	V _{DIFF}				V _{PVDD}	V _P
Power-Supply Rejection Ratio	PSRR	V _{DD} = from 2.5V to 5.5V	74	90		dB
		f _{IN} = 217Hz, 200mVpp		78		
		f _{IN} = 10kHz, 200mVpp		63		
Common-Mode Rejection Ratio	CMRR	-V _{PVDD} /2 ≤ V _{CM} ≤ +V _{PVDD} /2	70	86		ms
Output Voltage Swing	V _{OUT}	1kHz, 600Ω load, THD+N < 0.1%	3			V _{RMS}
		1kHz, R _L = 600Ω, V _{PVDD} = V _{SVDD} = 3.3V, THD+N < 0.1%			2.15	

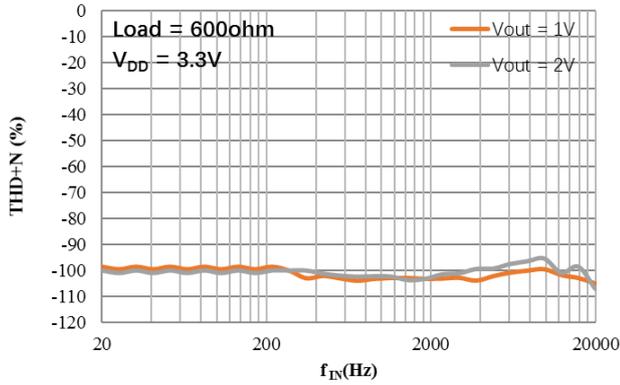
		1kHz, $R_L = 10k\Omega$, THD+N < 0.1%		3.5		
Output Power	P_{OUT}	$R_L = 16\Omega$, THD+N = 1%		110		mW
		$R_L = 32\Omega$, THD+N = 1%		125		
Total Harmonic Distortion Plus Noise	THD+N	1kHz, 22Hz to 22kHz BW, $V_{OUT} = 3V_{RMS}$, $R_L = 10k\Omega$		103		dB
		10kHz, 22Hz to 22kHz BW, $V_{OUT} = 3V_{RMS}$, $R_L = 10k\Omega$		100		
		1kHz, 22Hz to 22kHz BW, $V_{OUT} = 2V_{RMS}$, $R_L = 600\Omega$	80	105		
		10kHz, 22Hz to 30kHz BW, $V_{OUT} = 2V_{RMS}$, $R_L = 600\Omega$		105		
		1kHz, 22Hz to 22kHz BW, $P_{OUT} = 20mW$, $R_L = 32\Omega$		0.0021		%
Signal-to-Noise Ratio	SNR	$V_{OUT} = 3V_{RMS}$, THD+N = 0.1%, A-weighted, $R_L = 1k\Omega$		112.5		dB
		$V_{OUT} = 2V_{RMS}$, $V_{PVDD} = 3.3V$, THD+N = 0.1%, A-weighted, $R_L = 600\Omega$		109		
Output Noise Voltage	V_N	A-weighted, $R_{IN} = R_F = 10k\Omega$		7		μV
CrossTalk	CT	1kHz, $V_{OUT} = 3V_{RMS}$, $R_L = 10k\Omega$		-125		dB
		10kHz, $V_{OUT} = 3V_{RMS}$, $R_L = 10k\Omega$		-108		
		1kHz, $V_{OUT} = 2V_{RMS}$, $R_L = 600\Omega$, $V_{PVDD} = V_{SVDD} = 3.3V$		-123		
		10kHz, $V_{OUT} = 2V_{RMS}$, $R_L = 600\Omega$, $V_{PVDD} = V_{SVDD} = 3.3V$		-104		
		1kHz, $P_{OUT} = 20mW$, $R_L = 32\Omega$		-102		
		10kHz, $P_{OUT} = 20mW$, $R_L = 32\Omega$		-82		
Maximum Capacitive Load Drive	CL			470		pF
External Feedback Resistor Range	R_F		4.7	20	100	k Ω
Oscillator Frequency	f_{OSC}		450	500	550	kHz
Logic Input						
nSHDN Input Logic High	V_{IH}		1.4			V
nSHDN Input Logic Low	V_{IL}	Input Grounded, With or without load			0.4	V

*4: Depending on parts and PCB layout, characteristics may be changed.

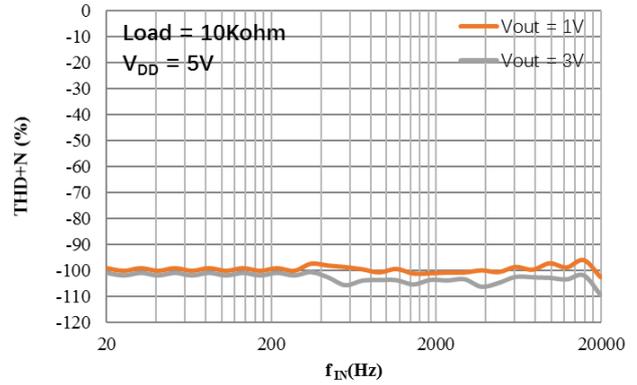
TYPICAL OPERATING CHARACTERISTICS

Condition: $T_a=25^{\circ}\text{C}$, $V_{DD} (= V_{PVDD} = V_{SVDD} = V_{SVD2}) = 5.0\text{V}$, $V_{PGND} = V_{SGND} = 0\text{V}$, $R_{IN} = R_F = 20\text{k}\Omega$, $C_{FLY} = 0.47\mu\text{F}$, $C_{PVDD} = C_{PVSS} = 1\mu\text{F}$, $C_{BIAS} = 0.1\mu\text{F}$, unless otherwise specified.

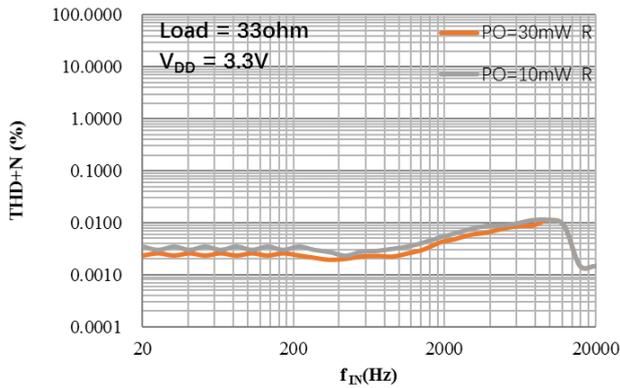
f_{IN} vs THD+N



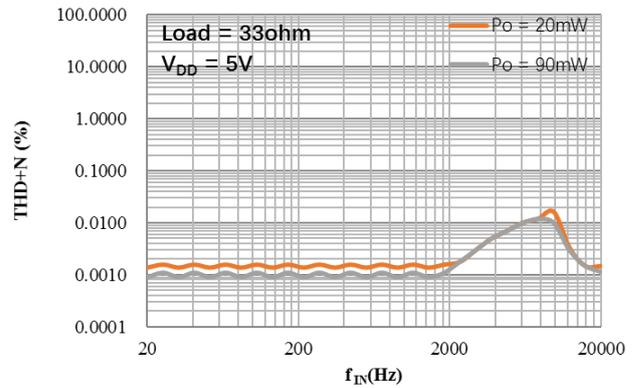
f_{IN} vs THD+N



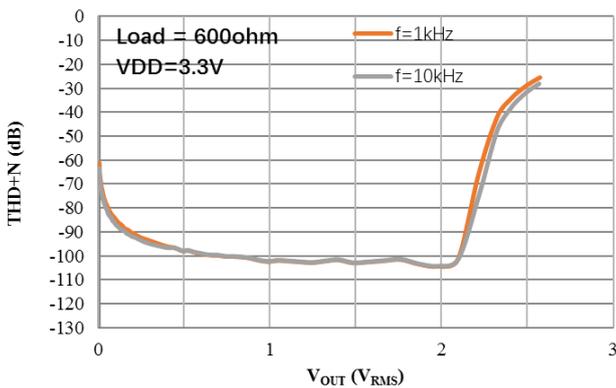
f_{IN} vs THD+N



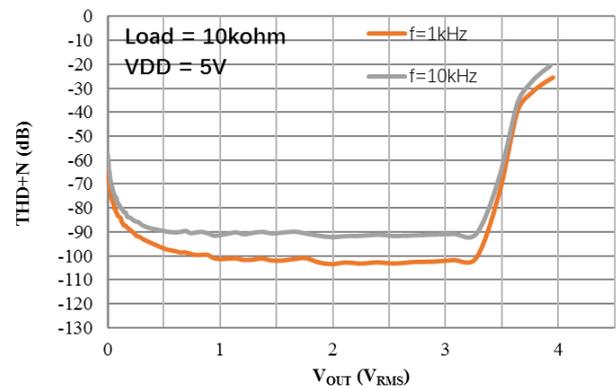
f_{IN} vs THD+N



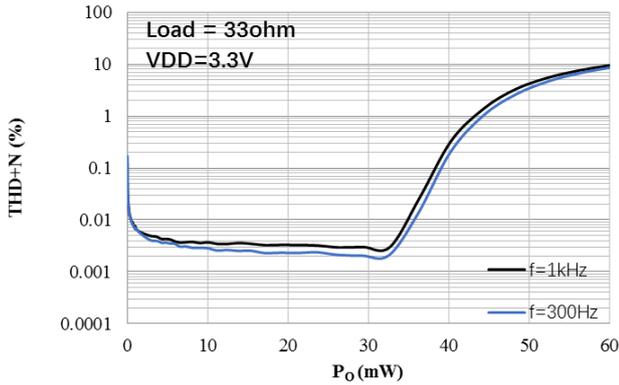
P_O vs THD+N



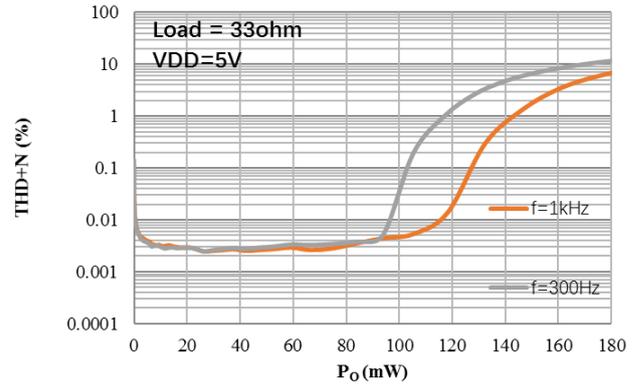
P_O vs THD+N



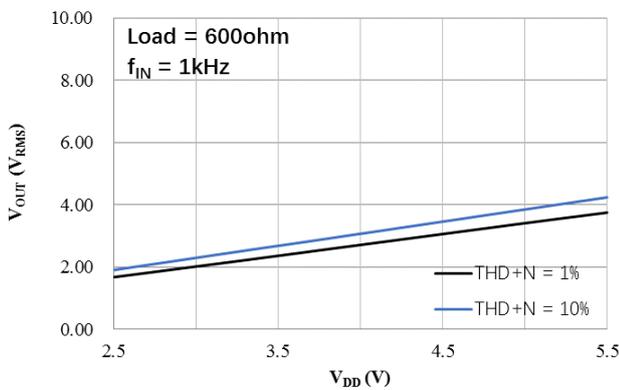
P_O vs THD+N



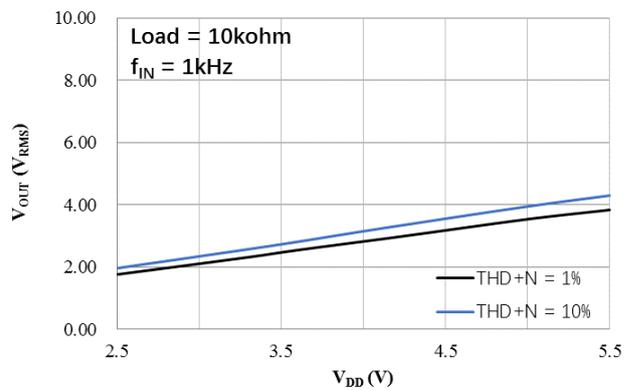
P_O vs THD+N



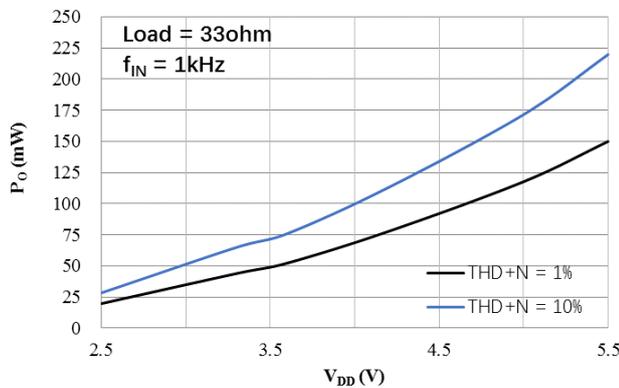
V_{DD} vs V_{OUT}



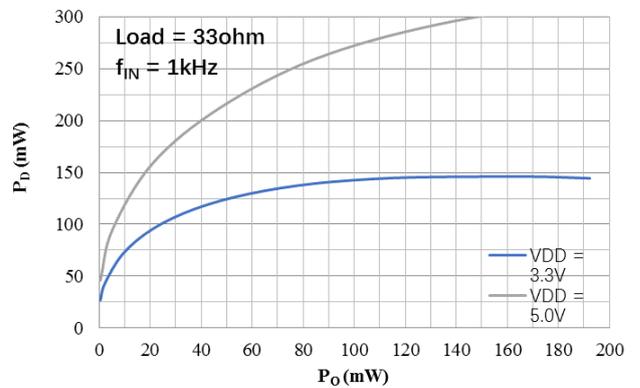
V_{DD} vs V_{OUT}



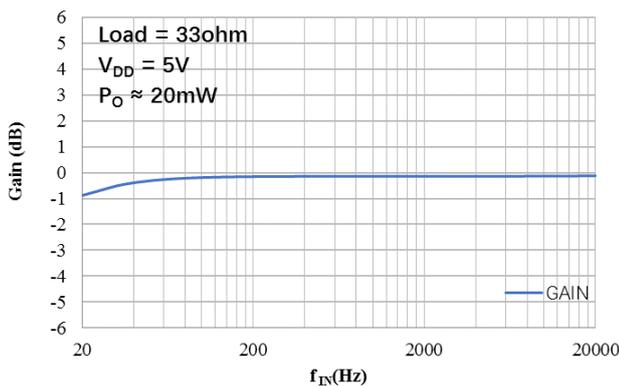
V_{DD} vs P_O



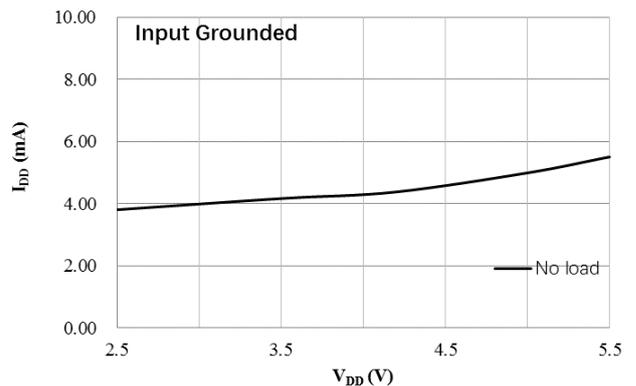
P_O (Output Power) vs P_D (Power Dissipation)



f_{IN} vs Gain



V_{DD} vs I_{DD}



APPLICATION INFORMATION

1. Detailed Description

The HT97220 is a fully differential input line driver/ headphone amplifier for set-top boxes, LCD TV, and home theater applications where audio fidelity is of primary importance. Power consumption of the amplifier is reduced while maintaining high SNR and THD+N performance. The HT97220 require external input and feedback resistors to set amplifier gain. For internal fixed gain of +6dB, it is only available if pre-booked. Output swings of 3VRMS with a 5V supply and 2VRMS with a 3.3V supply are perfect for line driver applications. High fidelity is maintained through the differential input connection. An output noise voltage of 7uVRMS allows for 112dB SNR when powered from 5V and 109dB SNR when powered from 3.3V. The IC has better than 90dB THD+N across the entire audio bandwidth.

The HT97220 operates from a single supply ranging from 2.5V to 5.5V. An on-chip charge pump inverts the positive supply (PVDD), creating an equal magnitude negative supply (PVSS). The headphone amplifiers operate from bipolar supplies with their outputs biased about PGND (Figure 1). The benefit of this PGND bias is that the amplifier outputs do not have a DC component, typically PVDD/2. The large DC-blocking capacitors required with conventional headphone amplifiers are unnecessary, thus conserving board space, reducing system cost, and improving frequency response. Output power of 125mW into 32Ω is achievable from a 5V supply. The device features an under-voltage lockout that prevents operation from an insufficient power supply and click-pop suppression that eliminates audible transients on startup and shutdown.

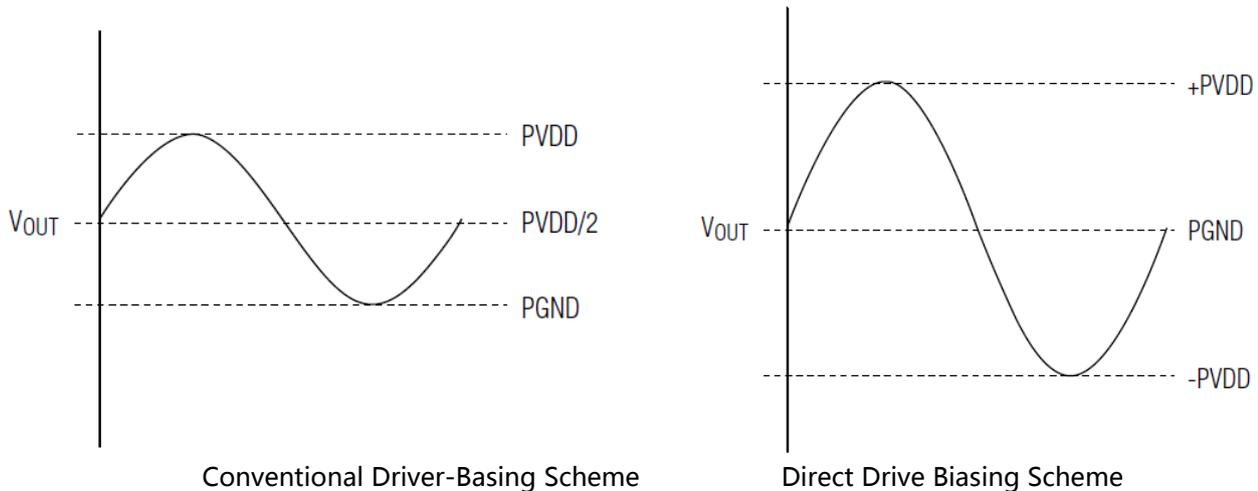


Fig. 1 Conventional Driver Output Waveform vs. HT97220 Output Waveform

2. Differential Input or Single-Ended Input

The IC can be configured as differential or single-ended input amplifiers (Figures 2 and 3), making it compatible with all codecs. A differential input offers improved noise immunity over a single-ended input. In devices such as cellular phones, high-frequency signals from the RF transmitter can couple into the amplifier's input traces. The signals appear at the amplifier's inputs as common-mode noise. A differential input amplifier amplifies the difference of the two inputs while signals common to both inputs are cancelled. The gain of the HT97220 is set by:

$$A_v = R_f/R_{IN}$$

The common-mode rejection ratio (CMRR) is limited by the external resistor matching, and if used, input capacitor matching at low frequencies. For example, the worst-case variation of 1% tolerant resistors results in

40dB CMRR, while 0.1% resistors result in 60dB CMRR. For best matching, use resistor arrays.

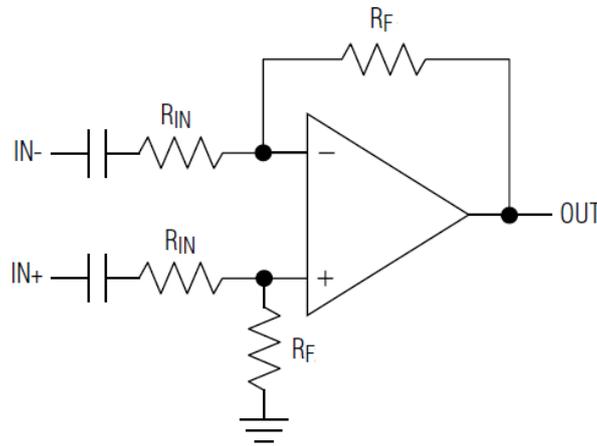


Fig. 2 Differential Input Configuration

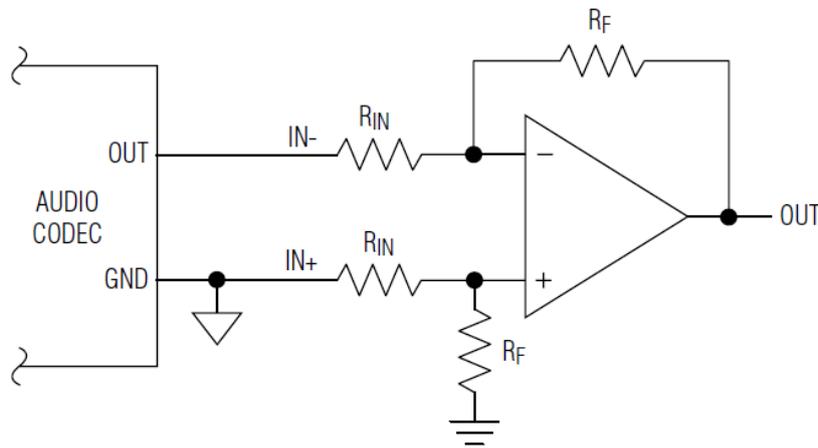


Fig. 3 Single-ended Input Configuration

3. Direct Drive

Conventional single-supply headphone amplifiers have their outputs biased about a nominal DC voltage (typically half the supply) for maximum dynamic range. Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both the headphone and the headphone amplifier.

HT97220 uses a charge pump to create an internal negative supply voltage, allowing the IC's outputs to be biased about PGND. With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220FF, typ.) tantalum capacitors, the IC charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier.

4. Input Filters

In addition to the cost and size disadvantages of DC-blocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal.

If input capacitors are used, input capacitor C_{IN} , in conjunction with input resistor R_{IN} , forms a high-pass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the

signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the high-pass filter is given by:

$$f_{-3dB} = 1/(2\pi R_{IN}C_{IN})$$

Setting f_{-3dB} too high affects the low-frequency response of the amplifier. Use capacitors with adequately low voltage coefficients, such as X7R ceramic capacitors with a high voltage rating. Capacitors with higher voltage coefficients result in increased distortion at low frequencies.

5. Bias Capacitor

Bypass BIAS with a 0.1uF capacitor to PGND. Do not connect external loads to BIAS.

6. Charge Pump

The HT97220 features a low-noise charge pump. The 500kHz switching frequency is well beyond the audio range and, thus, does not interfere with the audio signals. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. By limiting the switching speed of the charge pump, the di/dt noise caused by the parasitic bond wire and trace inductance is minimized. The IC requires a 0.47uF flying capacitor between C1P and C1N and a 1uF hold capacitor from PVSS to PGND.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range, select capacitors with an X7R dielectric.

The value of the flying capacitor (C_{FLY}) affects the charge pump's load regulation and output resistance. A C_{FLY} value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C_{FLY} improves load regulation and reduces the charge-pump output resistance to an extent. Above 1uF, the on-resistance of the switches and the ESR of C_{FLY} and C_{PVSS} dominate.

The hold capacitor value and ESR directly affect the ripple at PVSS. Use a low-ESR 1uF capacitor for C_{PVSS}.

7. Click-pop Suppression

The IC features click-pop suppression circuitry. When entering shutdown, the amplifier outputs are high impedance to ground. This scheme minimizes the energy present in the audio band.

8. Shutdown

The IC features a 1uA lower low-power shutdown mode that reduces power consumption. When the active-low shutdown mode is entered, the device's internal bias circuitry is disabled, the amplifier outputs go high impedance, and BIAS is driven to PGND. The HT97220 inputs are driven to PGND.

9. Amplifier Gain

The gain of the HT97220 amplifier is set externally. The gain is:

$$A_V = -R_F/R_{IN}$$

Choose feedback resistor values between the 4.7kΩ and 100kΩ range.

There's another version of HT97220 that has an internally fixed 6dB gain needs to be pre-booked.

10. Supply Bypassing

Proper power-supply bypassing ensures low-noise, low-distortion performance. Connect a 1uF ceramic capacitor from PVDD to PGND and a 1uF ceramic capacitor from SVDD to PGND. Add additional bulk capacitance as required by the application. Locate the bypass capacitor as close as possible to the device.:

11. PCB Layout and Grounding

Good PCB layout is essential for optimizing performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance and route heat away from the device. Good grounding improves audio performance, and prevents any digital switching noise from coupling into the audio.

Connect PGND and SGND together at a single point on the PCB. Connect all components associated with the charge pump (C_{FLY} and C_{PVSS}) to the PGND plane. Connect PVDD and SVDD together at the device. Place capacitors C_{FLY} and C_{PVSS} as close as possible to the device. Ensure the PCB layout is partitioned so that the large switching currents in the ground plane do not return through SGND and the traces and components in the audio signal path.

The IC is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes. Also, ensure a solid ground plane is used in multilayer PCB designs.

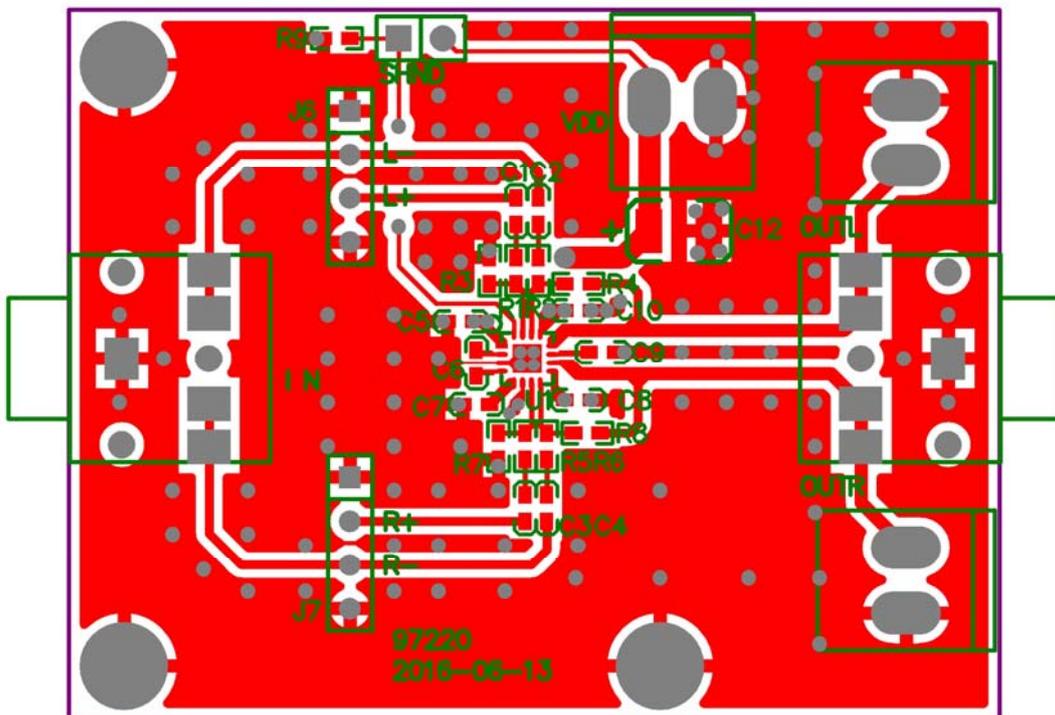


Fig.4 Top View of HT97220 Demo Board PCB Layout

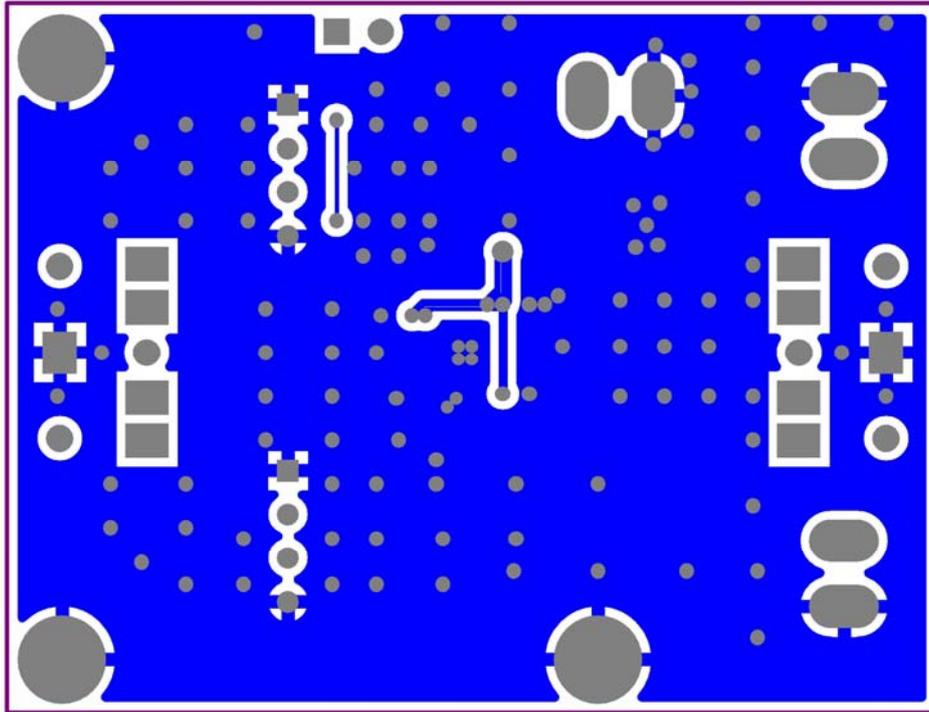
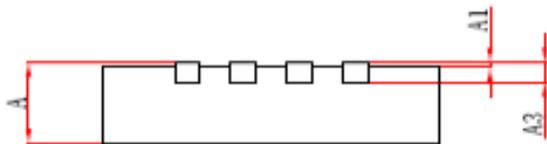
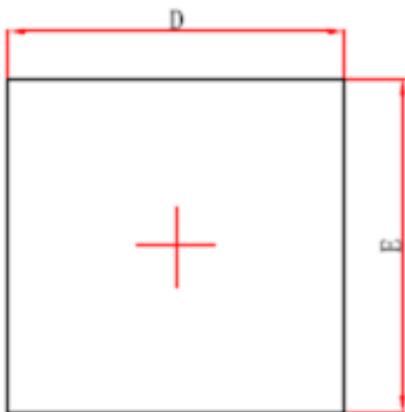
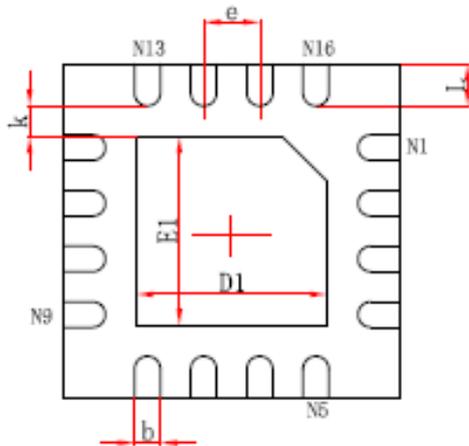


Fig.5 Bottom View of HT97220 Demo Board PCB Layout

■ PACKAGE OUTLINE



Symbol	Dimension in Millimeters (mm)	
	Min.	Max.
A	0.700	0.900
A1	0.000	0.050
A3	0.203(REF)	
D	2.900	3.100
E	2.900	3.100
D1	1.600	1.800
E1	1.600	1.800
k	0.200MIN	
b	0.180	0.300
e	0.500TYP	
L	0.300	0.500

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